Name of the Department: Electronics Communication and Instrumentation Engineering
Name of the Department Research and Education Centre (DREC):

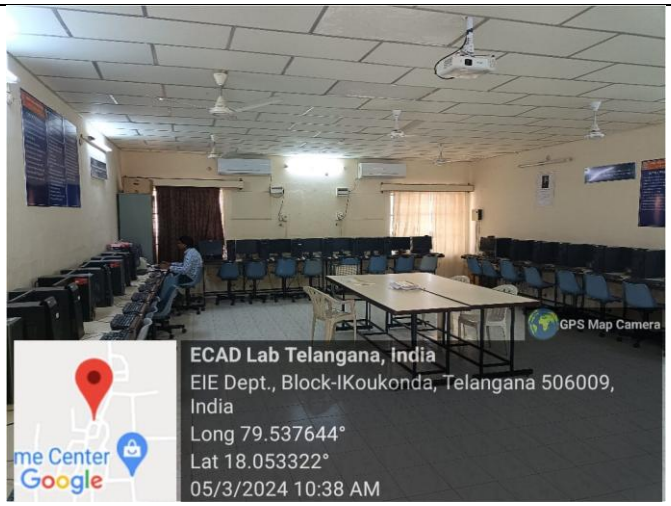
Research & Education Centre	**Room No.**
VLSI	**B-I-219**

About the DREC:	A Research and Education Centre focused on VLSI (Very Large Scale Integration) typically engages in activities related to the design, development, and education in the field of integrated circuits and systems. VLSI technology involves the integration of a large number of transistors and other electronic components into a single chip, enabling the creation of complex and powerful electronic systems. Here are some key aspects that such a center may cover: **Research in VLSI Design:** • Developing innovative and efficient VLSI design methodologies. • Exploring new architectures and technologies to improve the performance and energy efficiency of integrated circuits. **Education and Training:** • Offering courses, workshops, and training programs in VLSI design and related areas. • Providing hands-on experience with design tools, simulation, and chip fabrication processes. **Publications and Conferences:** • Publishing research papers in reputable journals and presenting findings at conferences to contribute to the academic community. • Organizing conferences or workshops to bring together experts, researchers, and industry professionals to share knowledge and advancements. **Innovation and Prototyping:** • Encouraging innovation by supporting projects that push the boundaries of VLSI technology. • Providing resources and expertise to help researchers and students prototype their designs. **Interdisciplinary Research:** • Collaborating with researchers from other disciplines, such as computer science, electrical engineering, and materials science, to address complex challenges in integrated circuit design.

Primary functions of the DREC:	A VLSI (Very Large Scale Integration) Research and Education Centre typically focuses on research, development, and education in the field of VLSI design. Here are the primary functions of such a center: • Conducting cutting-edge research in VLSI design methodologies, algorithms, and tools. • Exploring novel techniques for optimizing and enhancing the performance of integrated circuits. • Developing new architectures and design paradigms to meet the evolving demands of electronic systems. • Offering courses and training programs to educate students, researchers, and industry professionals in VLSI design. • Providing hands-on experience with VLSI design tools, simulation techniques, and programming to build practical skills. • Supervising student projects and internships related to VLSI design. • Providing a platform for students to gain practical experience and contribute to ongoing research activities.

Major equipment available in DREC:

S. No.	Name of the Major Equipment	Description of equipment	Cost
1.	SPARTAN 6 ATLYS Boards	The Spartan-6 LX45 is optimized for high-performance logic and offers: • 6,822 slices, each containing four 6-input LUTs and eight flip-flops • 2.1Mbits of fast block RAM • four clock tiles (eight DCMs & four PLLs) • six phase-locked loops • 58 DSP slices • 500MHz+ clock speeds	2,00,000.00
2.	Digilent Nexys 4DDR FPGA KITS	**FPGA Part #** XC7A100T-1CSG324C **Logic Slices :** 15,850 (4 6-input LUTs & 8 flip-flops each) **Block RAM :** 4,860 Kbits **Clock Tiles :** 6 (each with PLL) **DSP Slices :** 240 **Internal clock :** 450 MHz+ **DDR2:** 128 MiB **Cellular RAM :**16MB **Ethernet :** 10/100 PHY	1,95,880.00
3.	Lenovo	Intel G630 Dual Core - G630, Processor – Intel (R) Pentium(R) @ 2.80GHz	5,70,000.00
4.	Acer	Pentium(R) Dual-Core - E6600, Processor – Intel (R) Pentium(R) @ 3.06GHz,	74,250.00

Picture of DREC	

Software available in DREC:

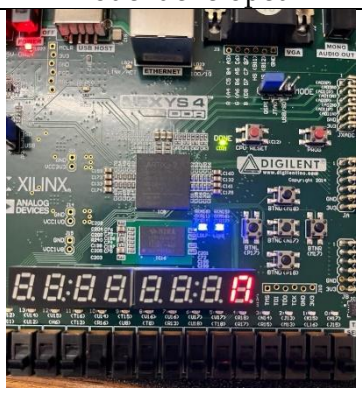
S. No.	Name of the Software	Purpose of Software	Cost (in Rs.)
1.	MATLAB Math works Campus wide suite	Ph.D., PG & UG	1,93,637.00
2.	Xilinx Vivado Design Suite	Ph.D., PG & UG	2,00,000.00
3.	MATLAB R2012,	Ph.D., PG & UG	5,66,936.00
4.	Dev-C++	UG	-
5.	JAVA	UG	-

Types of projects / research carried out with description:

S. No.	Name of the Project / Research carried out in the DREC	Outcome of Project / Research carried out
1.	Research- Design of 0.8 V, 22 nm DG-FinFET based efficient VLSI multiplexers	Published an article in SCI Journal. Link to Published article: https://www.sciencedirect.com/science/article/abs/pii/S0026269221000707
2.	Research: A 16 nm finfet circuit with triple function as digital multiplexer, active-high and active-low output decoder for high-performance sram architecture	Published an article in SCI Journal. Link to Published article: https://iopscience.iop.org/article/10.1088/1361-6641/ac77ae/meta

3.	Research: Design of efficient 22 nm, 20-FinFET full adder for low-power and high-speed arithmetic units	Published an article in SCI Journal. Link to Published article: https://link.springer.com/article/10.1007/s12633-022-02073-z
4.	PG student Project: Simulation and synthesis of UART through FPGA Zedboard for IoT applications	Published a conference paper in IEEE Xplore: https://ieeexplore.ieee.org/abstract/document/9752556
5.	UG student Project: Implementation of parallel multiplier based on Booth computing method using FPGA	https://ieeexplore.ieee.org/abstract/document/9752479 Published a conference paper in IEEE Xplore:

Photographs of working models/ application software developed with description:

S. No.	Name of the Working model developed in the DREC	Details of working model developed
	UG student Project: Implementation of parallel multiplier based on Booth computing method using FPGA	

Details of Faculty incharge for Research and Education Centre: (Photo, Contact details)

Name of the Faculty Incharge, DREC	Contact details
	Phone No: 99121 55777 Mail ID: bj.eie@kitsw.ac.in

HoD-EIE & Programme Head-ECI
(Dr. M. Raghu Ram)